IN THE CLAIMS

Claims 40-58 are pending in the application with claims 40, 48, and 56 amended herein.

Claims 1-39 (canceled).

40. (currently amended) Integrated circuitry comprising:

a semiconductive substrate;

an electrically insulating layer over the semiconductive substrate; ~~and~~

a series of alternating first and second conductive lines spaced and positioned laterally adjacent one another directly over the insulating layer, the first conductive lines and the second conductive lines having respective line tops;[[,]] and ~~being electrically isolated from one another laterally by~~

intervening insulating spacers laterally between the first and second conductive lines, the spacers having respective spacer tops that are substantially coplanar with at least some of the first and second conductive line tops, the first conductive lines being electrically isolated from the second conductive lines, and the series of first conductive lines or the series of second conductive lines providing cross-talk shielding for the other series.

41. (previously presented) The integrated circuitry of claim 40 wherein at least some of the individual laterally adjacent first and second conductive lines are disposed directly on the electrically insulating layer.

42. (previously presented) The integrated circuitry of claim 40 wherein the first conductive lines have a substantially common lateral cross sectional shape and the second conductive lines have a substantially common lateral cross sectional shape, the first conductive lines' lateral cross sectional shape being different from the second conductive lines' lateral cross sectional shape.

43. (previously presented) The integrated circuitry of claim 40 wherein the first and second conductive lines constitute the same materials.

44. (previously presented) The integrated circuitry of claim 40 wherein the first and second conductive lines constitute different materials.

45. (previously presented) The integrated circuitry of claim 40 wherein the first conductive lines predominately comprise undoped polysilicon and the second conductive lines predominately comprise metal.

46. (previously presented) The integrated circuitry of claim 40 wherein the first conductive lines predominately comprise doped polysilicon and the second conductive lines predominately comprise metal.

47. (previously presented) The integrated circuitry of claim 40 comprising a plurality of the series of the first and second conductive lines at multiple elevations relative to the substrate.

48. (currently amended) Integrated circuitry comprising:

a semiconductive substrate;

a layer of electrically insulating material over the semiconductive substrate; and

a series of alternating first and second conductive lines directly over the layer of insulating material, the first and second conductive lines having respective lateral widths and being spaced and positioned laterally adjacent one another; and ~~, the first conductive lines and the second conductive lines being electrically isolated and separated from one another laterally by~~

intervening strips of insulating material laterally between the first and second conductive lines, the insulating material only having respective individual insulating material lateral widths that are substantially less than the lateral widths of any of the first and second conductive lines, the first conductive lines being electrically isolated from the second conductive lines, and none of the first and second conductive lines overlapping any immediately laterally adjacent first or second conductive lines.

49. (previously presented) The integrated circuitry of claim 48 wherein each of the first and second conductive lines are disposed on and in contact with the layer of insulating material.

50. (previously presented) The integrated circuitry of claim 48 wherein the first conductive lines have a substantially common lateral cross sectional shape and the second conductive lines have a substantially common lateral cross sectional shape, the first conductive lines' lateral cross sectional shape being different from the second conductive lines' lateral cross sectional shape.

51. (previously presented) The integrated circuitry of claim 48 wherein the first and second conductive lines constitute the same materials.

52. (previously presented) The integrated circuitry of claim 48 wherein the first and second conductive lines constitute different materials.

53. (previously presented) The integrated circuitry of claim 48 wherein the first conductive lines predominately comprise undoped polysilicon and the second conductive lines predominately comprise metal.

54. (previously presented) The integrated circuitry of claim 48 wherein the first conductive lines predominately comprise doped polysilicon and the second conductive lines predominately comprise metal.

55. (previously presented) The integrated circuitry of claim 48 comprising a plurality of the series of the first and second conductive lines at multiple elevations relative to the substrate.

56. (currently amended) Integrated circuitry comprising:

a semiconductive substrate;

an electrically insulative borophosphosilicate glass (BPSG) layer over the semiconductive substrate;

a series of first conductive polysilicon lines over the BPSG layer, the first series conductive lines having individual pairs of respective sidewalls;

electrically insulative oxide material ~~over~~ on and in contact with respective first series conductive lines, a top of the insulative oxide material over at least some of the first series conductive lines defining a first plane;

a plurality of insulative oxide sidewall spacer pairs, individual spacer pairs being on respective sidewall pairs of individual first series conductive lines and being connected with the electrically insulative oxide material over the respective individual first series conductive lines;

individual first series conductive lines being effectively insulated by the BPSG layer, the respective sidewall spacer pairs, and the respective insulative oxide material; and

a series of second conductive aluminum-containing lines having respective line tops at least some of which define a second plane that is coplanar with said first plane, the series of second conductive lines being over the BPSG layer and electrically isolated from the first conductive lines.

57. (previously presented) The integrated circuitry of claim 56, wherein first series conductive lines have elevational thicknesses in a range from 2000 Angstroms to 10,000 Angstroms.

58. (previously presented) The integrated circuitry of claim 56, wherein individual second series conductive lines have substantially a common lateral cross sectional shape.

Claims 59-69 (canceled).